

Differences between FEB8 and FEB24 prototypes

The new FEB24 prototype design incorporates several new features, which do not exist in the FEB8 prototypes. The following is a list of the new features and changes implemented in the FEB24.

1. **A new 10-bit ADC.** The Analog Devices AD875 ADC chip is replaced with the Texas Instrument TLC876 10-bit ADC. The new ADC has an internal S&H circuitry and lesser power consumption. TLC876 doesn't have overflow and underflow bits in the output data format as AD875 does. These bits will be permanently set to zero in the event data word. In order to recognize overflow and underflow status if necessary, one can use TLC876 truth table that shows 3FF hex (all one's) value for overflow and 000 hex value (all zeros) for underflow input conditions respectively. The new ADC chip also does not have an output test feature as AD875 chip does.
2. **New LED indicators.** Four additional LED's are added to the board. The new LED's indicate the following signals:
 - Err 1 LED (red, static) indicates Level 1 FIFO overflow
 - TrgOR LED (green, 100 ms)) indicates Trigger OR signal
 - TRUN LED (green, static) indicates TRUN bit status
 - PRUN LED (green, static) indicates PRUN bit status
3. **New FIFO full registers.** In addition to Level 1 FIFO empty flag registers, three new Level 1 FIFO full flag 8-bit registers are added to the FEB24. These registers will be used for diagnostic purposes if error condition occurs. They replace old ADC test control registers implemented in the FEB8. An updated FEB24 address map follows.

Table 1. FEB registers VME address map.

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment
02	PTEN	WTEN	TGT5	TGT4	TGT3	TGT2	TGT1	TGT0	Trigger Gate and Test
04	CE8	CE7	CE6	CE5	CE4	CE3	CE2	CE1	Channel 1-8 ENBL
06	CE16	CE15	CE14	CE13	CE12	CE11	CE10	CE9	Channel 9-16 ENBL
08	CE24	CE23	CE22	CE21	CE20	CE19	CE18	CE17	Channel 17-24 ENBL
0A	EF8	EF7	EF6	EF5	EF4	EF3	EF2	EF1	L1 FIFO 1-8 EFs
0C	EF16	EF15	EF14	EF13	EF12	EF11	EF10	EF9	L1 FIFO 9-16 EFs
0E	EF24	EF23	EF22	EF21	EF20	EF19	EF18	EF17	L1 FIFO 17-24 EFs
10	BF8	BF7	BF6	BF5	BF4	BF3	BF2	BF1	ADC FIFO 1-8 EFs
12	BF16	BF15	BF14	BF13	BF12	BF11	BF10	BF9	ADC FIFO 9-16 EFs
14	BF24	BF23	BF22	BF21	BF20	BF19	BF18	BF17	ADC FIFO 17-24 EFs
16	X	X	X	E1 test	PEN	WEN	PRUN	TRUN	RUN Control register
18	FF8	FF7	FF6	FF5	FF4	FF3	FF2	FF1	L1 FIFO 1-8 FFs
1A	FF16	FF15	FF14	FF13	FF12	FF11	FF10	FF9	L1 FIFO 9-16 FFs
1C	FF24	FF23	FF22	FF21	FF20	FF19	FF18	FF17	L1 FIFO 17-24 FFs
1E	X	X	AD5	AD4	AD3	AD2	AD1	AD0	ADC Pipeline Control
20	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC1 CRS0
22	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC1 CSR1
24	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC1 CSR2
26	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC1 CSR3
40	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC2 CRS0
42	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC2 CSR1
44	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC2 CSR2
46	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC2 CSR3

60	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC3 CRS0
62	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC3 CSR1
64	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC3 CSR2
66	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC3 CSR3
80	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC4 CRS0
82	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC4 CSR1
84	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC4 CSR2
86	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC4 CSR3
A0	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC5 CRS0
A2	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC5 CSR1
A4	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC5 CSR2
A6	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC5 CSR3
C0	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC6 CRS0
C2	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC6 CSR1
C4	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC6 CSR2
C6	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC6 CSR3